DESIGN OF A BCD TO SEVEN SEGMENT CODE CONVERTER USING PSEUDO NMOS LOGIC

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Introduction:

A seven-segment display is used to display digits from 0 to 9

These displays are more frequently used when we have to obtain output only in the form of digits like a digital clock or digital speedometer etc.

This seven segment LED display has seven individual LEDs and these displays are available in two forms one is the common cathode display and the other one is common anode display.

In common cathode display all the seven LEDs cathodes are tied together and anodes are individually controlled through the display controller IC to display the required digit.

Similarly in common anode display all the seven LEDs anodes are tied together and cathodes are individually controlled.

In this seven segment LED display along with the seven segments there is another eighth segment for the purpose of representing the decimal point but most of the times it is not used.

Logic circuit Design:

Here in this project the circuit is designed only for valid BCD codes i.e. 0-9.

Invalid BCD codes are taken as don’t cares i.e. A-F.

a

f b

g

e c

d

The truth table is taken as follows,

For Common cathode display where ABCD is the BCD code (A is MSB)

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Digit | A | B | C | D | a | b | c | d | e | f | g |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 2 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| 3 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 |
| 4 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 5 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 |
| 6 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 7 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| 8 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 9 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |
| A | 1 | 0 | 1 | 0 | X | X | X | X | X | X | X |
| B | 1 | 0 | 1 | 1 | X | X | X | X | X | X | X |
| C | 1 | 1 | 0 | 0 | X | X | X | X | X | X | X |
| D | 1 | 1 | 0 | 1 | X | X | X | X | X | X | X |
| E | 1 | 1 | 1 | 0 | X | X | X | X | X | X | X |
| F | 1 | 1 | 1 | 1 | X | X | X | X | X | X | X |

Now, in order to design the logic circuit for controlling this this seven-segment display we need to solve the k map for each of the seven functions a, b , c , d , e , f ,g.

Solving K-map for function a:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| AB\CD | 00 | 01 | 11 | 10 |
| 00 | 1 | 0 | 1 | 1 |
| 01 | 0 | 1 | 1 | 1 |
| 11 | x | x | x | x |
| 10 | 1 | 1 | x | x |

a= A + C + BD + B’D’

on following the similar procedure for solving the k-maps for the other functions also we obtain the following final expressions

b=A + B’ + C’D’ + CD

c=C’ + D +B

d=A + CD’ + B’D’ + B’CD + BC’D

e=B’D’ + CD’

f=A + BC’ + A’C’D’ + BCD’

g=A + BC’ + CD’ + B’C

now in order to implement these functions using the pseudo nmos logic we need to convert these expressions to expressions that come out as an output in complementary form like below

These conversions are required in order to reduce one inverter for each function.

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

a= A’C’ (B + D) (B’ + D’)

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

b= A’B (C + D) (C’ + D’)

\_\_\_\_

c= CD’B

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

d= A’ (C’ + D) (B + D) (B + C’ + D’) (B’ + C + D’)

\_\_\_\_\_\_\_\_\_\_\_\_\_

e= (B +D) (C’ + D)

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

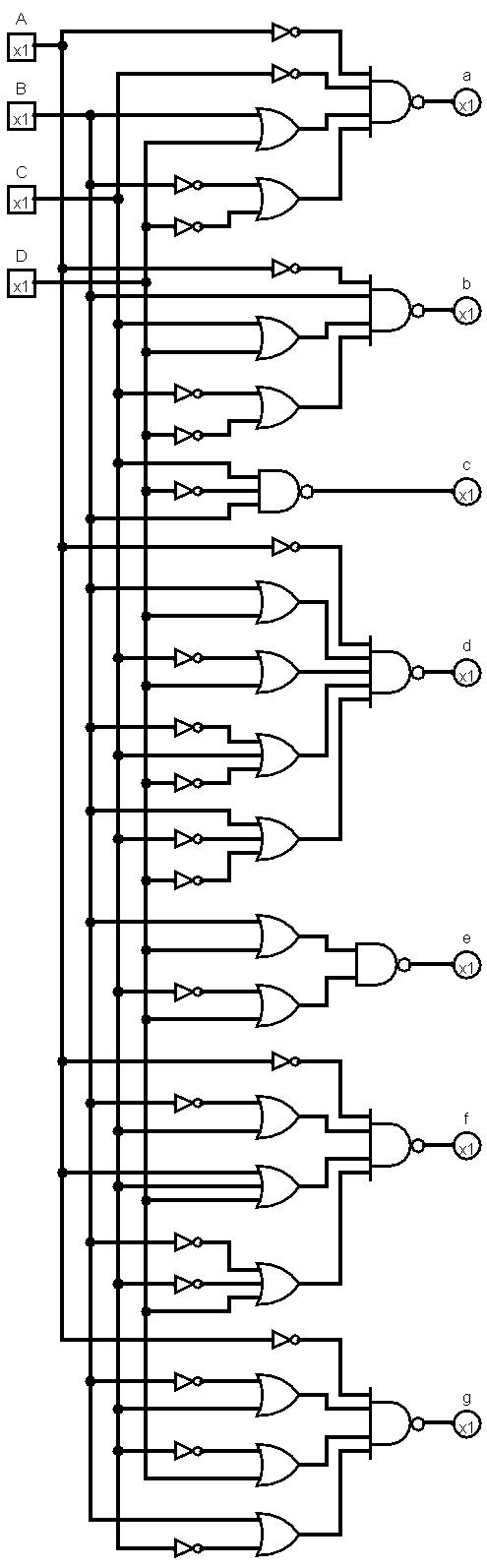
f= A’ (B’ + C) (A + C + D) (B’ + C’ +D)

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

g= A’ (B’ + C) (C’ + D) (B + C’)

In this project the IC design is completed up to Schematic and testing by giving appropriate inputs.

Now, the logic circuit is taken as follows



SCHEMATIC DESIGN:

Here there are 7 outputs (a, b, c, d, e, f, g) and four inputs (A, B, C, D)

Here one subcircuit is used for taking inputs and also the complements of these inputs by making use of inverters.

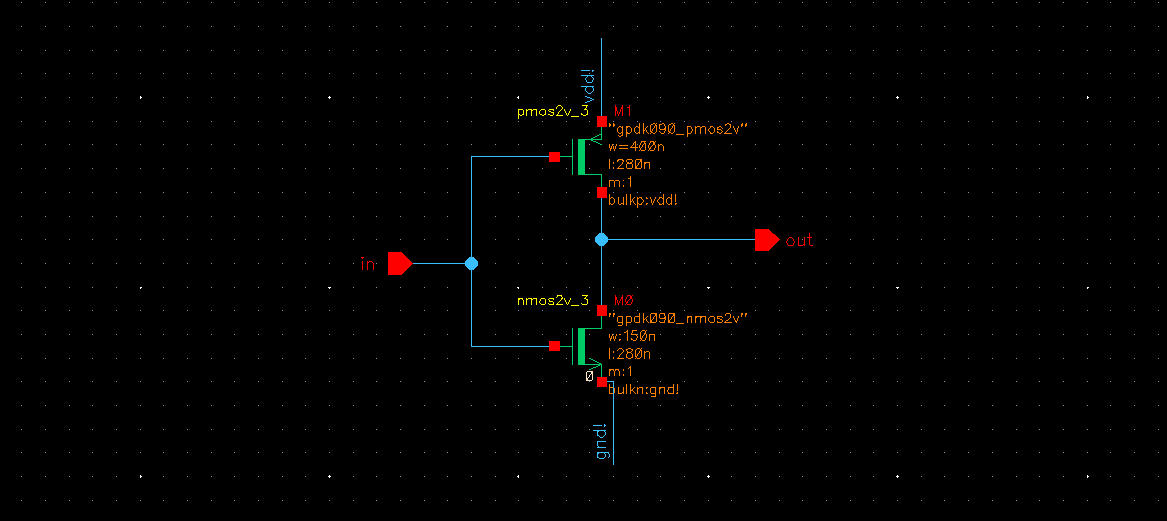
The inverter is designed in such a way that the W/L ratio of the pmos is 2.5 times the W/L ratio of nmos transistor for the purpose of proper switching voltage (0.5 VDD).

The schematic of the basic inverter used in this project is as shown below.

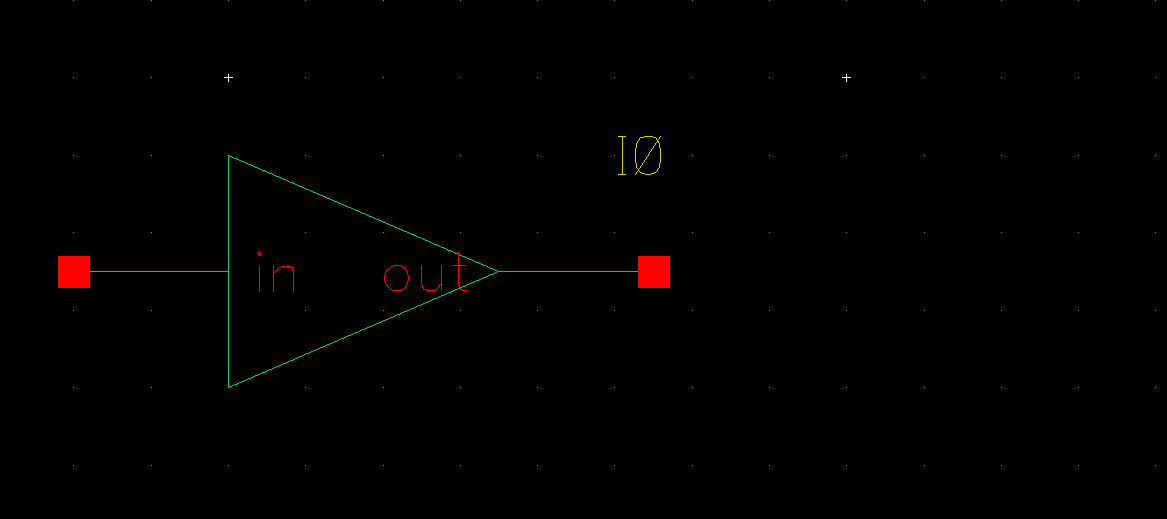
Transistor dimensions table:

|  |  |  |
| --- | --- | --- |
| Transistor | Width (nm) | Length (nm) |
| M0 (nmos pull down) | 150 | 280 |
| M1 (pmos pull up) | 400 | 280 |

INVERTER:

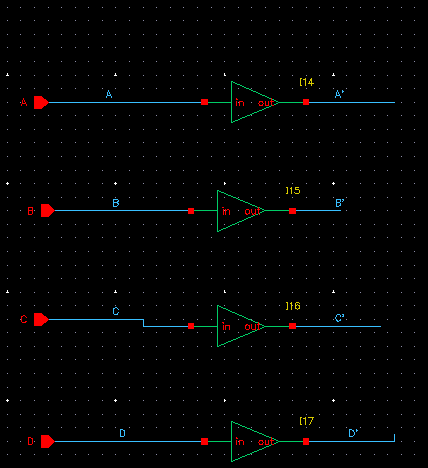


INVERTER SYMBOL:



Now by making use of these inverters the inputs subcircuit is designed as shown below.

INPUTS SUBCIRCUIT:



Now each of the output an individual subcircuit is designed by using pseudo nmos logic where single pmos is used as pull up network and nmos transistors are used according to the required logic as pull-down network.

Here an additional pin CKCA’ is used to select the common cathode (CACK’=0) or common anode (CKCA’=1) operation of the IC. For this purpose xor gates are employed to take the final output.

For these xor gates one of the inputs is CKCA’ and the other input is the output of the subcircuit whenever the CKCA’ is logic ‘0’ it will allow the outputs to pass without any changes and achieving the common cathode mode of operation.

Also, whenever the CKCA’ is logic ‘1’ it will give the complements of the outputs of the subcircuit, by this it achieves the common anode mode of operation.

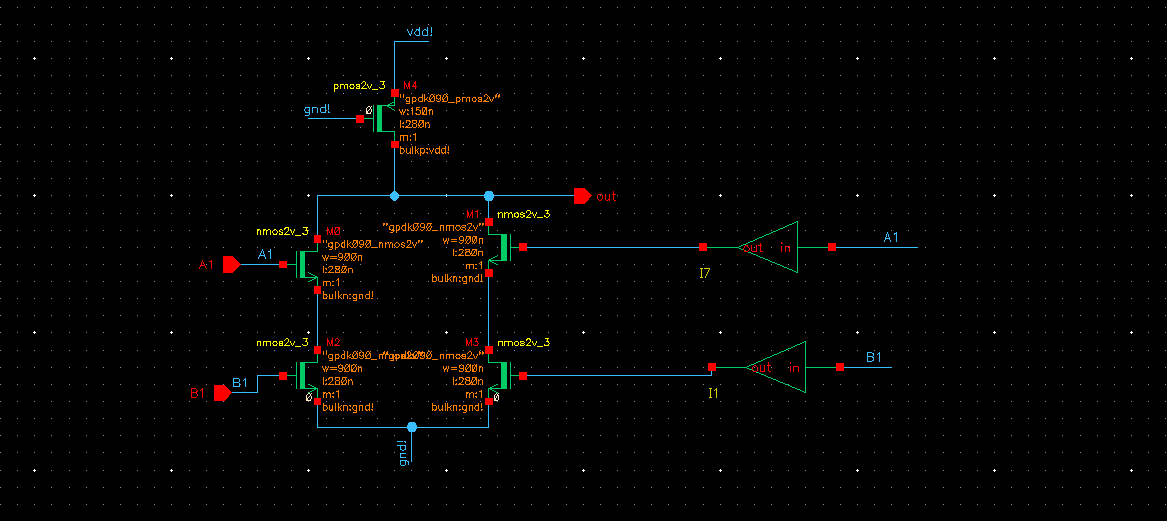
The exor gate is also designed by using pseudo nmos logic, for obtaining the good enough noise margin the W/L ratio of the NMOS transistors are taken 6 times the W/L ratio of the PMOS transistor.

The schematic of the basic xor used in this project is as shown below.

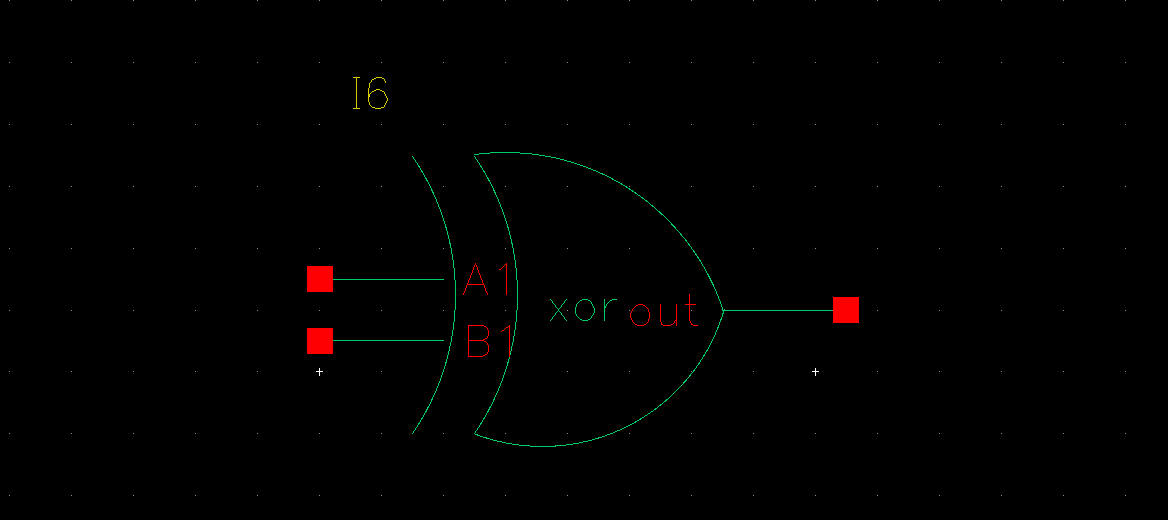
Transistor dimensions table:

|  |  |  |
| --- | --- | --- |
| Transistor | Width (nm) | Length (nm) |
| M0 (nmos pull down) | 900 | 280 |
| M1 (nmos) | 900 | 280 |
| M2 (nmos) | 900 | 280 |
| M3 (nmos) | 900 | 280 |
| M4 (pmos pull up) | 150 | 280 |

SCHEMATIC XOR GATE:



XOR SYMBOL:

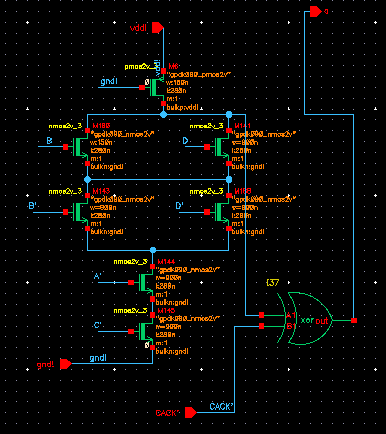


Now by making use of these inverters and the pseudo NMOS logic the subcircuit for output a is designed as shown below.

Transistor dimensions table:

|  |  |  |
| --- | --- | --- |
| Transistor | Width (nm) | Length (nm) |
| All nmos transistors | 900 | 280 |
| All pmos transistors | 150 | 280 |

SCHEMATIC OF SUBCIRCUIT a:



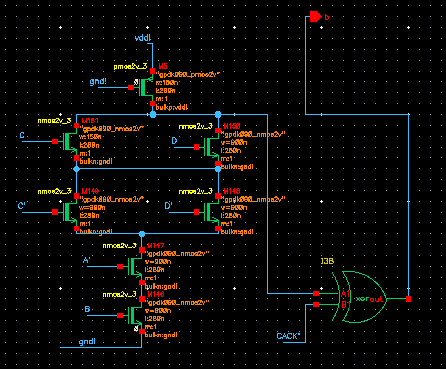
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a= A’C’ (B + D) (B’ + D’)

Transistor dimensions table:

|  |  |  |
| --- | --- | --- |
| Transistor | Width (nm) | Length (nm) |
| All nmos transistors | 900 | 280 |
| All pmos transistors | 150 | 280 |

SCHEMATIC OF SUBCIRCUIT b:



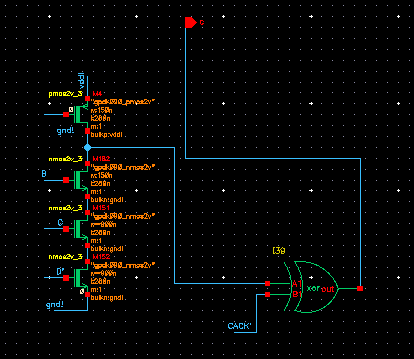
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b= A’B (C + D) (C’ + D’)

Transistor dimensions table:

|  |  |  |
| --- | --- | --- |
| Transistor | Width (nm) | Length (nm) |
| All nmos transistors | 900 | 280 |
| All pmos transistors | 150 | 280 |

SCHEMATIC OF SUBCIRCUIT c:



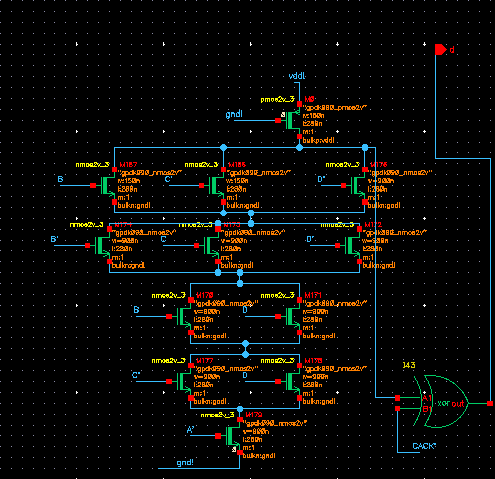
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c= CD’B

Transistor dimensions table:

|  |  |  |
| --- | --- | --- |
| Transistor | Width (nm) | Length (nm) |
| All nmos transistors | 900 | 280 |
| All pmos transistors | 150 | 280 |

SCHEMATIC OF SUBCIRCUIT d:



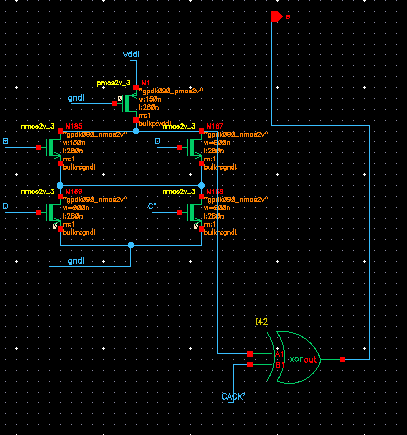
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d= A’ (C’ + D) (B + D) (B + C’ + D’) (B’ + C + D’)

Transistor dimensions table:

|  |  |  |
| --- | --- | --- |
| Transistor | Width (nm) | Length (nm) |
| All nmos transistors | 900 | 280 |
| All pmos transistors | 150 | 280 |

SCHEMATIC OF SUBCIRCUIT e:



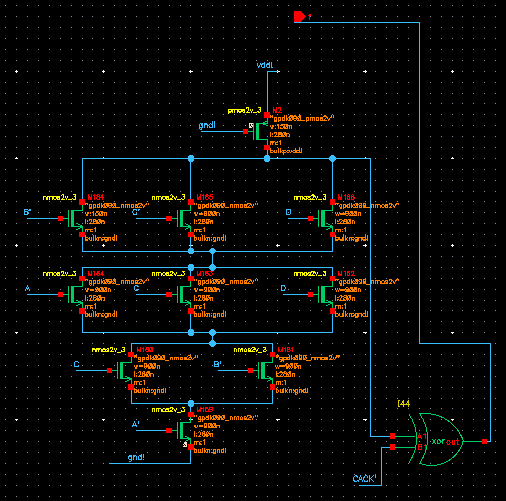
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e= (B +D) (C’ + D)

Transistor dimensions table:

|  |  |  |
| --- | --- | --- |
| Transistor | Width (nm) | Length (nm) |
| All nmos transistors | 900 | 280 |
| All pmos transistors | 150 | 280 |

SCHEMATIC OF SUBCIRCUIT f:



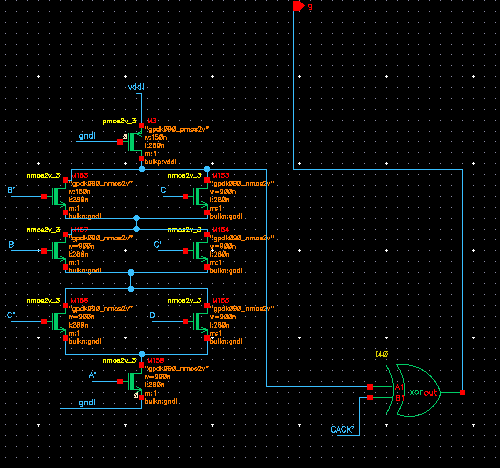
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f= A’ (B’ + C) (A + C + D) (B’ + C’ +D)

Transistor dimensions table:

|  |  |  |
| --- | --- | --- |
| Transistor | Width (nm) | Length (nm) |
| All nmos transistors | 900 | 280 |
| All pmos transistors | 150 | 280 |

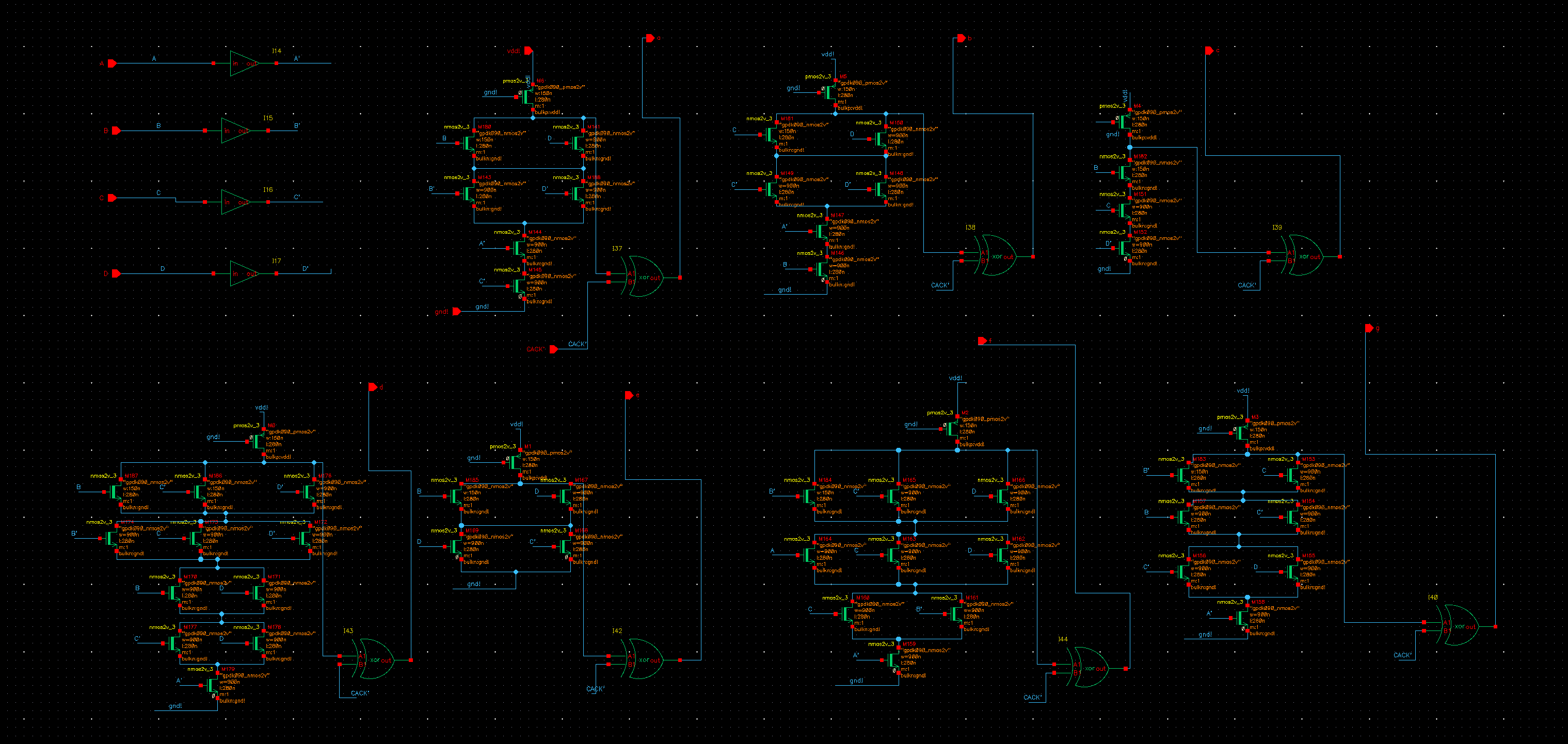
SCHEMATIC OF SUBCIRCUIT g:



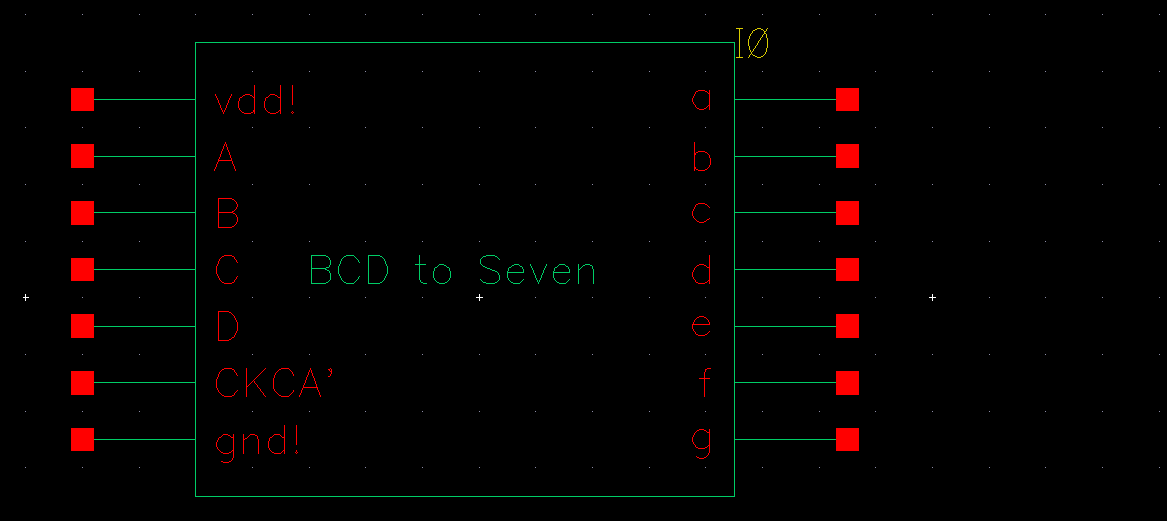
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g= A’ (B’ + C) (C’ + D) (B + C’)

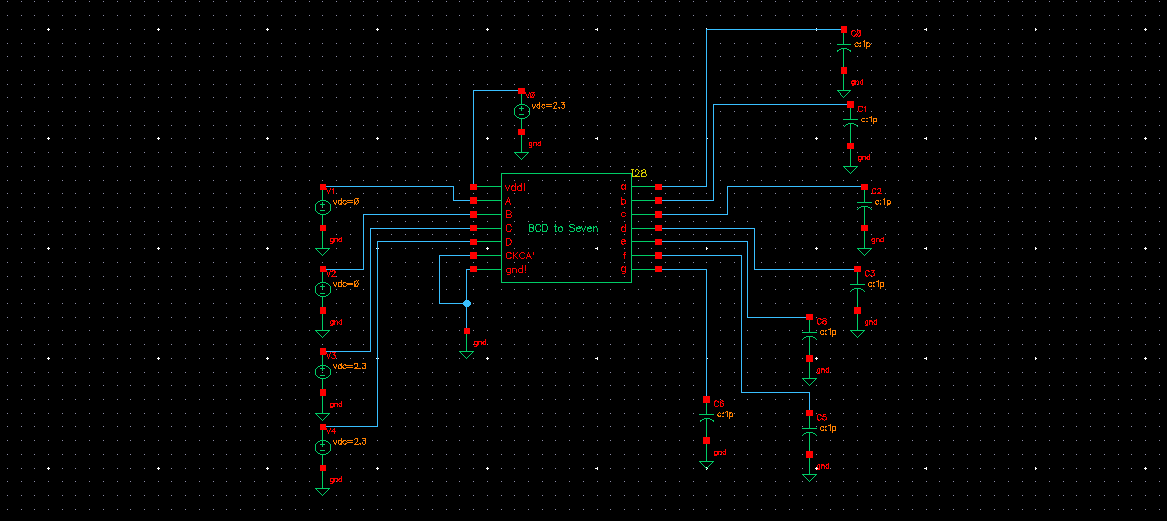
THE ENTIRE DESIGN:



SYMBOL OF THE BCD TO SEVEN SEGMENT CODE CONVERTER IC:



THE TESTBENCH:



The circuit treats any greater than 2V as logic ‘1’ and any value less than 300mv as logic ‘0’.

The vdd for the circuit is 2.3V.

INPUTS AND OUTPUTS:

For testing the circuit, the test input is given as by giving CKCA’ as logic ‘0’ to obtain common cathode outputs.

Input outputs required

A B C B a b c d e f g

0 0 1 1 1 1 1 1 0 0 1

a

f b

g

e c

d

Obtained output waveforms:

